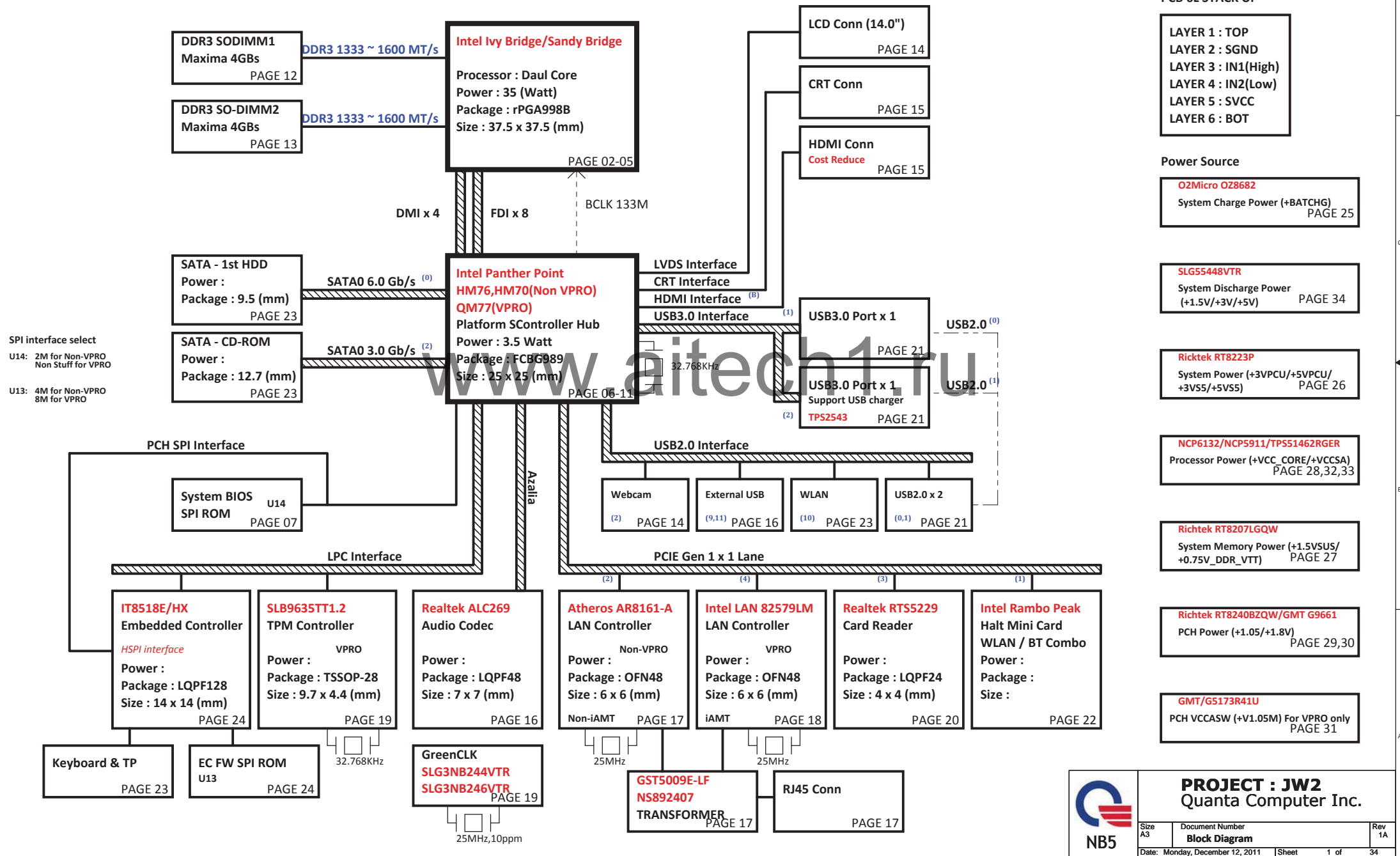
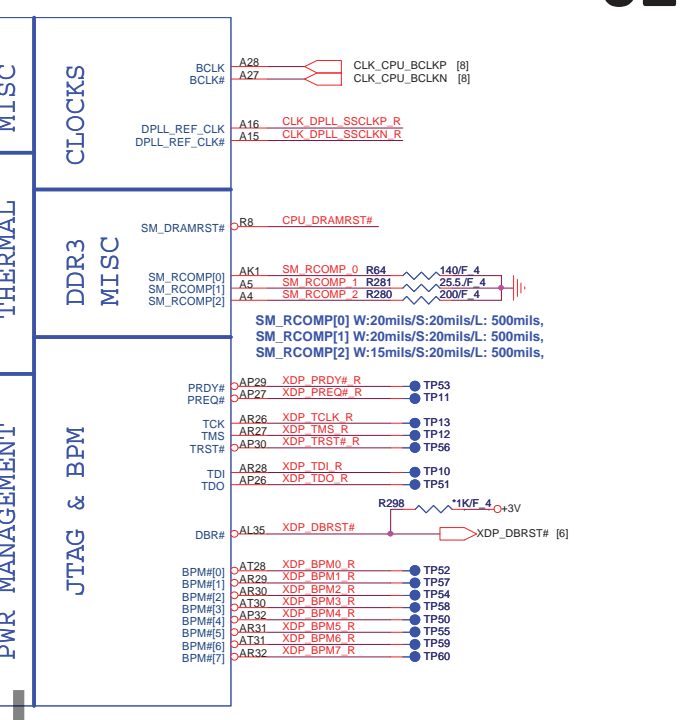


JW2 UMA (14.0") Intel Chief River Block Diagram

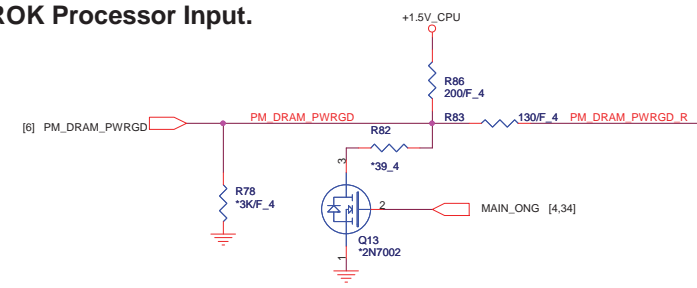




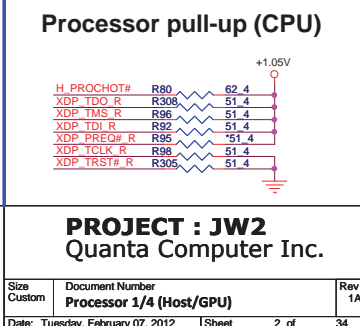
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SM_DRAMPWROK Processor Input.

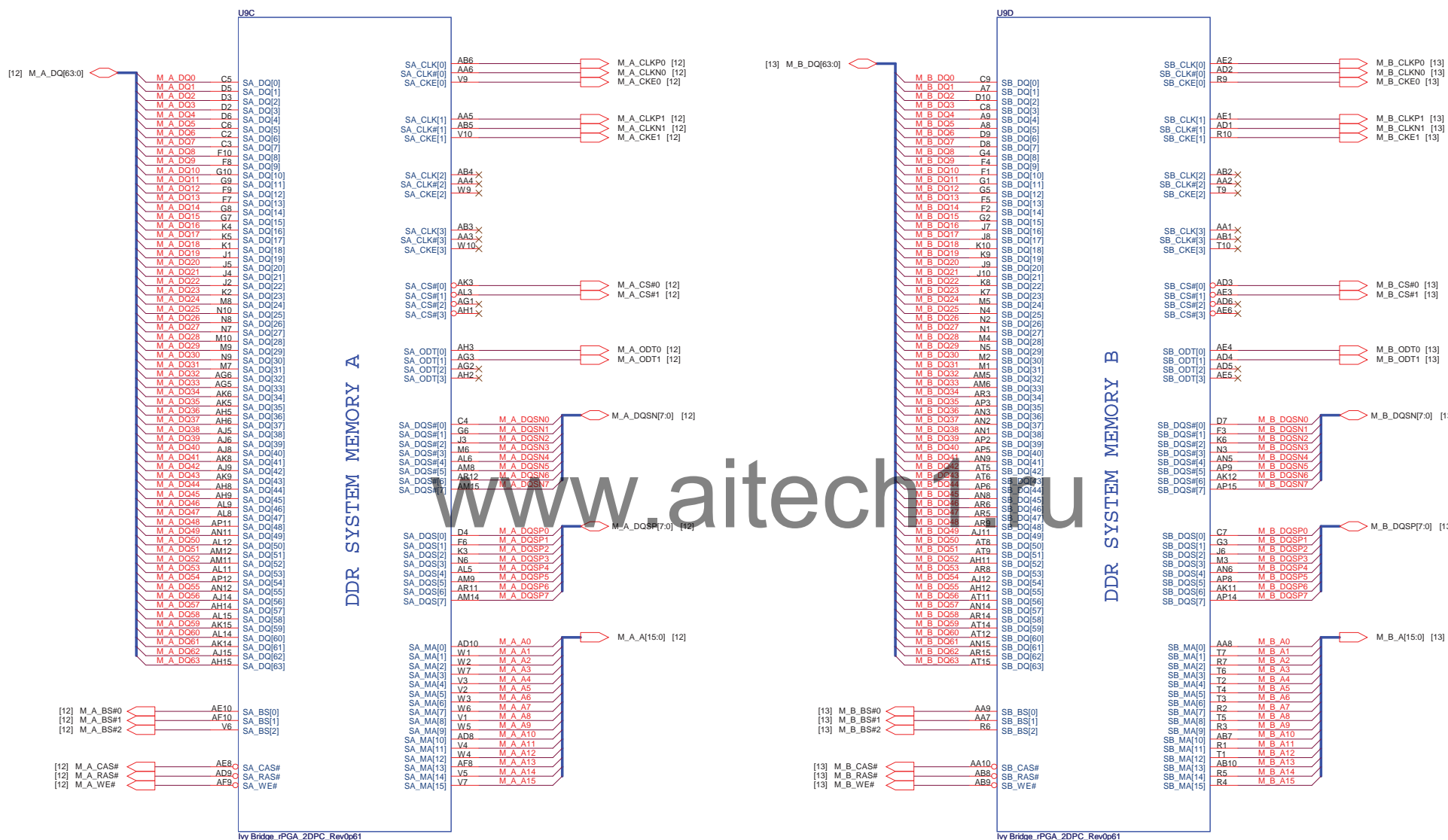
+1.5V_CPU



[6,7,8,9,10,12,13,14,15,16,17,19,20,22,23,24,29,32,34] +3V
[6,7,8,9,10,14,19,22,24,26,29,30,34] +3VS₅
[4,10,22] +1.5V_{CPU}
[4,6,7,8,10,19,24,29,32] +1.05V



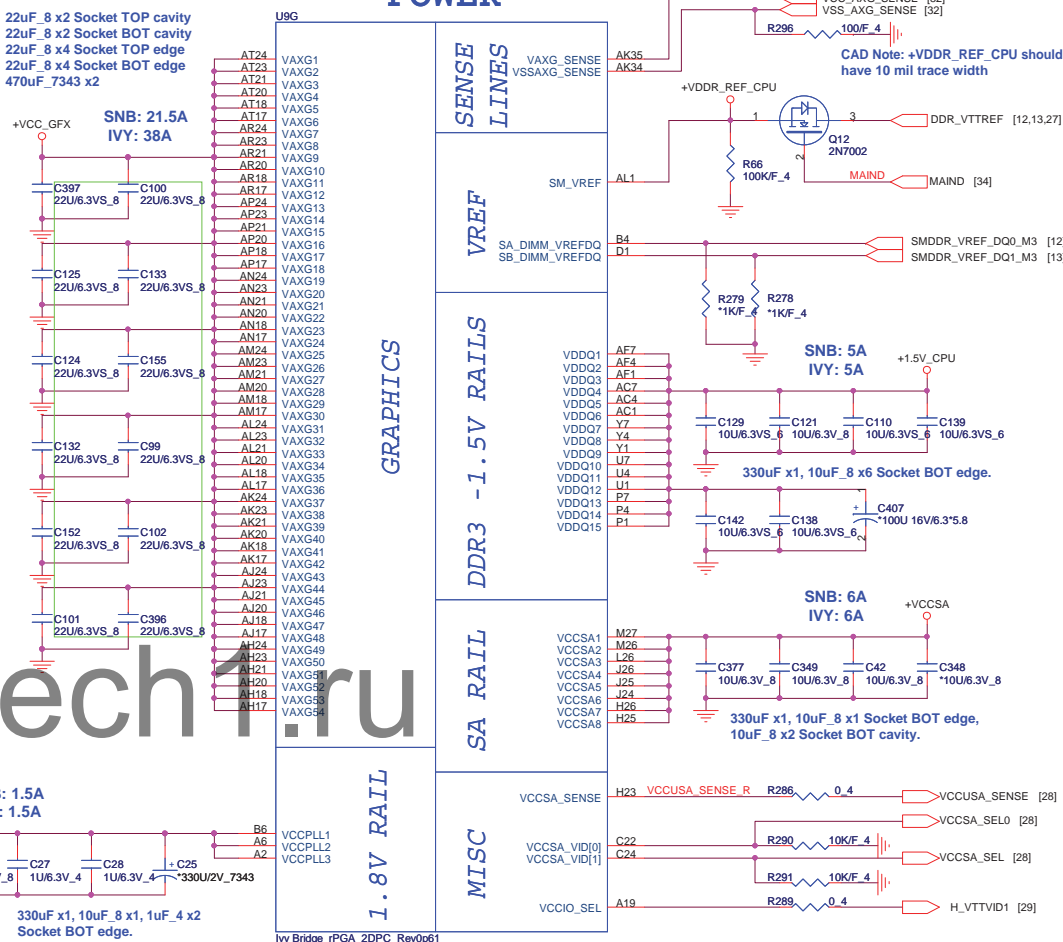
Ivy Bridge Processor (DDR3)



POWER



POWER



Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor
close to V_D

SVID CLK

SVID CLK

SVID DATA

SVID ALERT

VR_SVID_CLK VR SVID_CLK [32]

+1.05V B Test SVID DATA

Place PU resistor $\frac{1}{2}$ sec

Place PU resistor close to CPU **SVID ALER**

H_CPU_SVIDALRT# R72 43.4 MB_SVID_ALERT# [2]

	2
--	---

CPU VDDQ

PROJECT : JW2
Quanta Computer Inc.



Size Custom	Document Number Processor 3/4 (Power)	Revised
Date: Tuesday, February 07, 2012	Sheet 4 of 34	

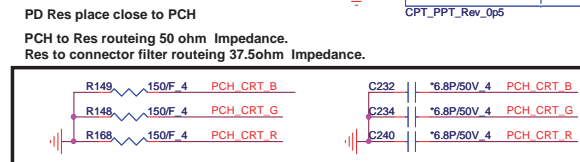
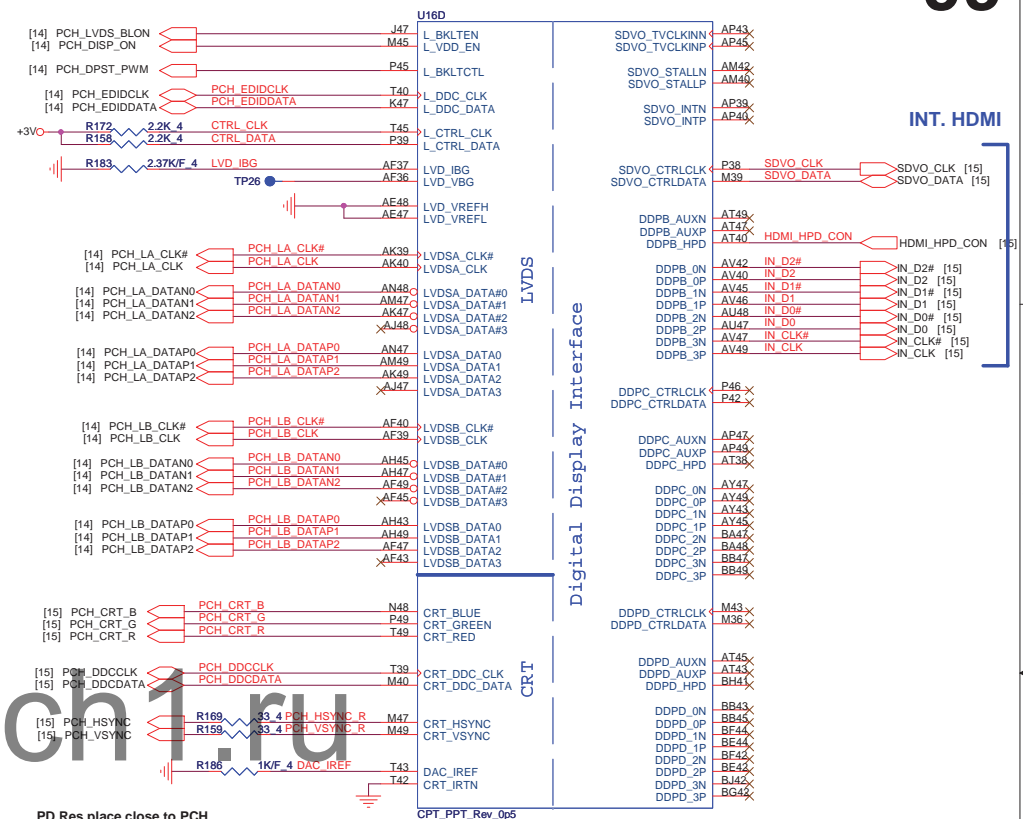
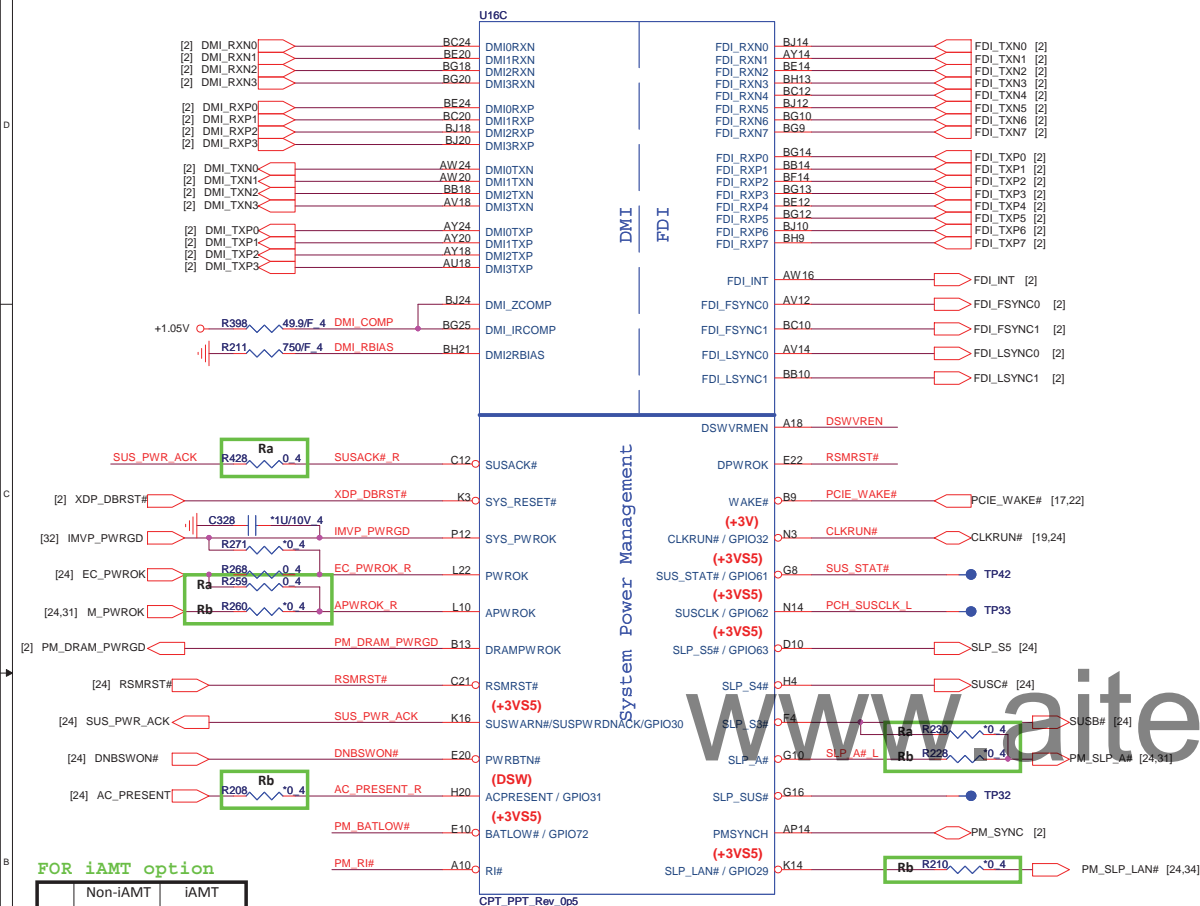


Size Custom	Document Number Processor 4/4 (Ground)	Rev 1A
Date: Thursday, December 08, 2011	Sheet 5 of	34

Cougar Point/Panther Point (DMI,FDI,PM)

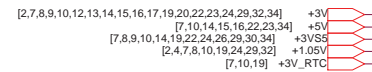
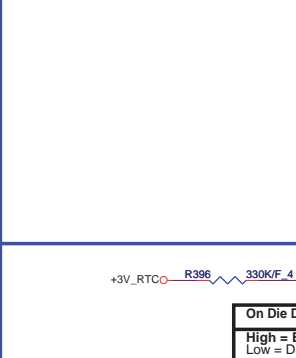
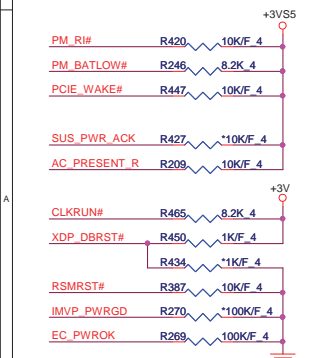
Cougar Point/Panther Point (LVDS,DDI)

06



PCH Pull-high/low(CLG)

System PWR_OK(CLG)



PROJECT : JW2
Quanta Computer Inc.

NB5

Size Custom

Document Number
PCH 1/6 (Host/Display)

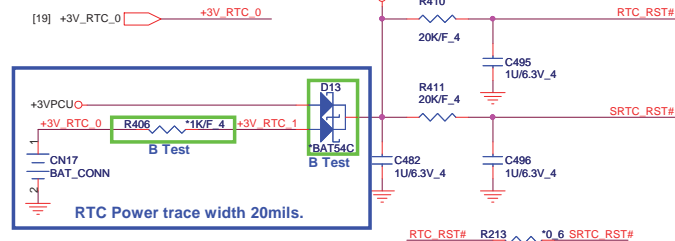
Rev 1A

Date: Tuesday, February 07, 2012

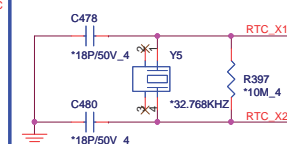
Sheet 6 of 34



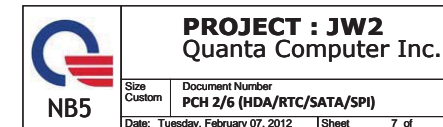
DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.



RTC Clock 32.768KHz

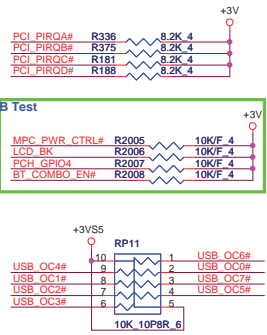


Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104H)
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DFHS08FS023

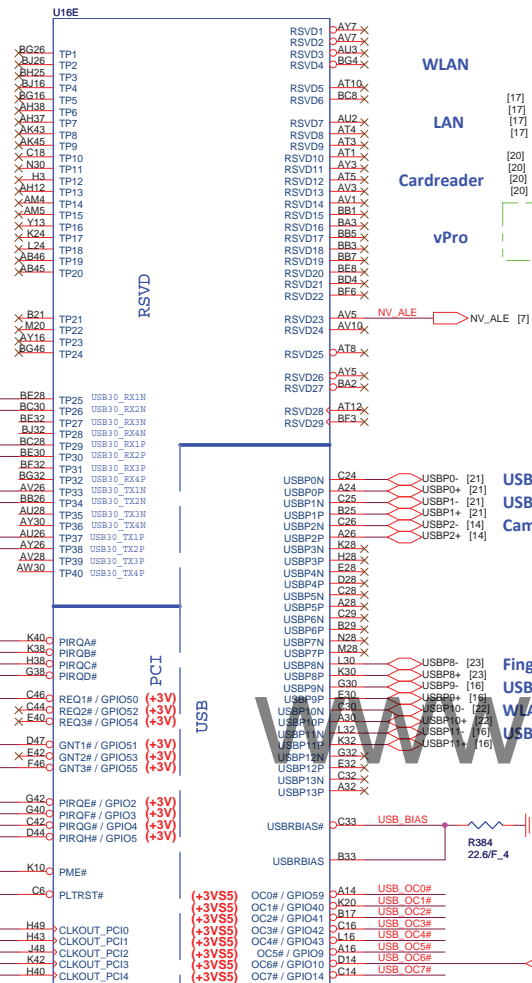


Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>0</td><td>SPI</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	0	LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

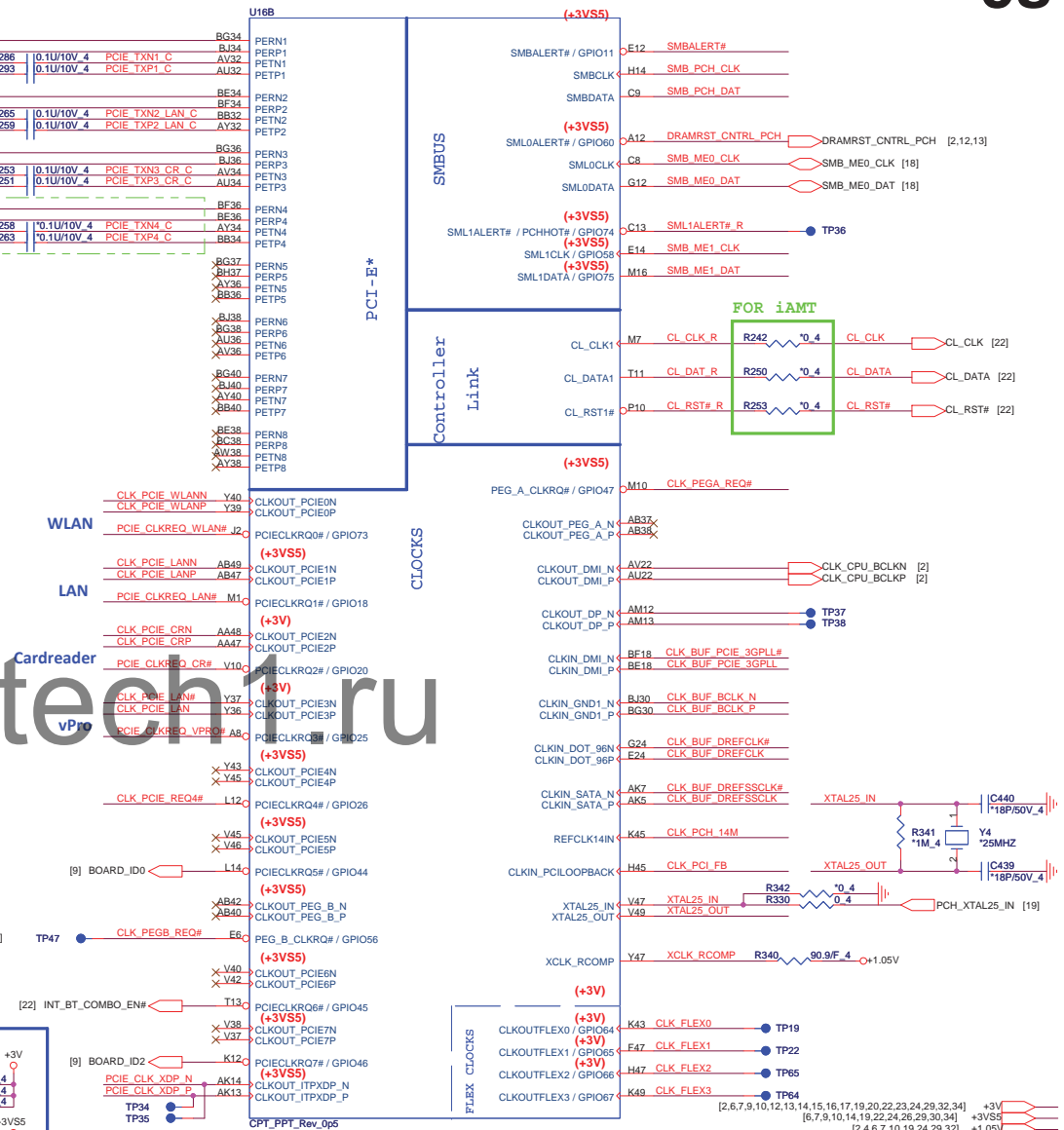
PCI/USBOC# Pull-up(CLG)



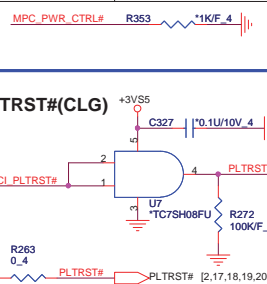
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



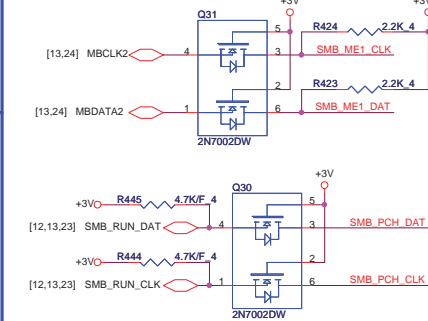
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



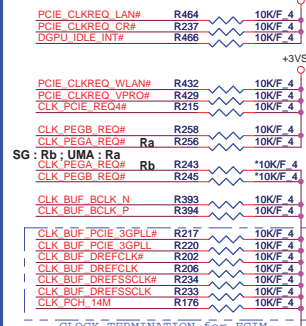
MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)



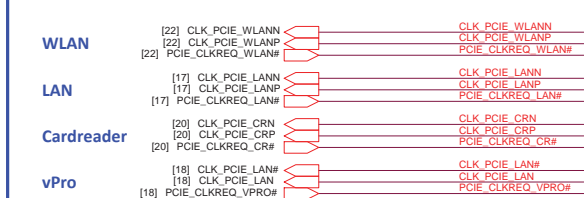
SMBus/Pull-up(CLG)



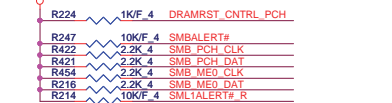
CLK_REQ/Strap Pin(CLG)



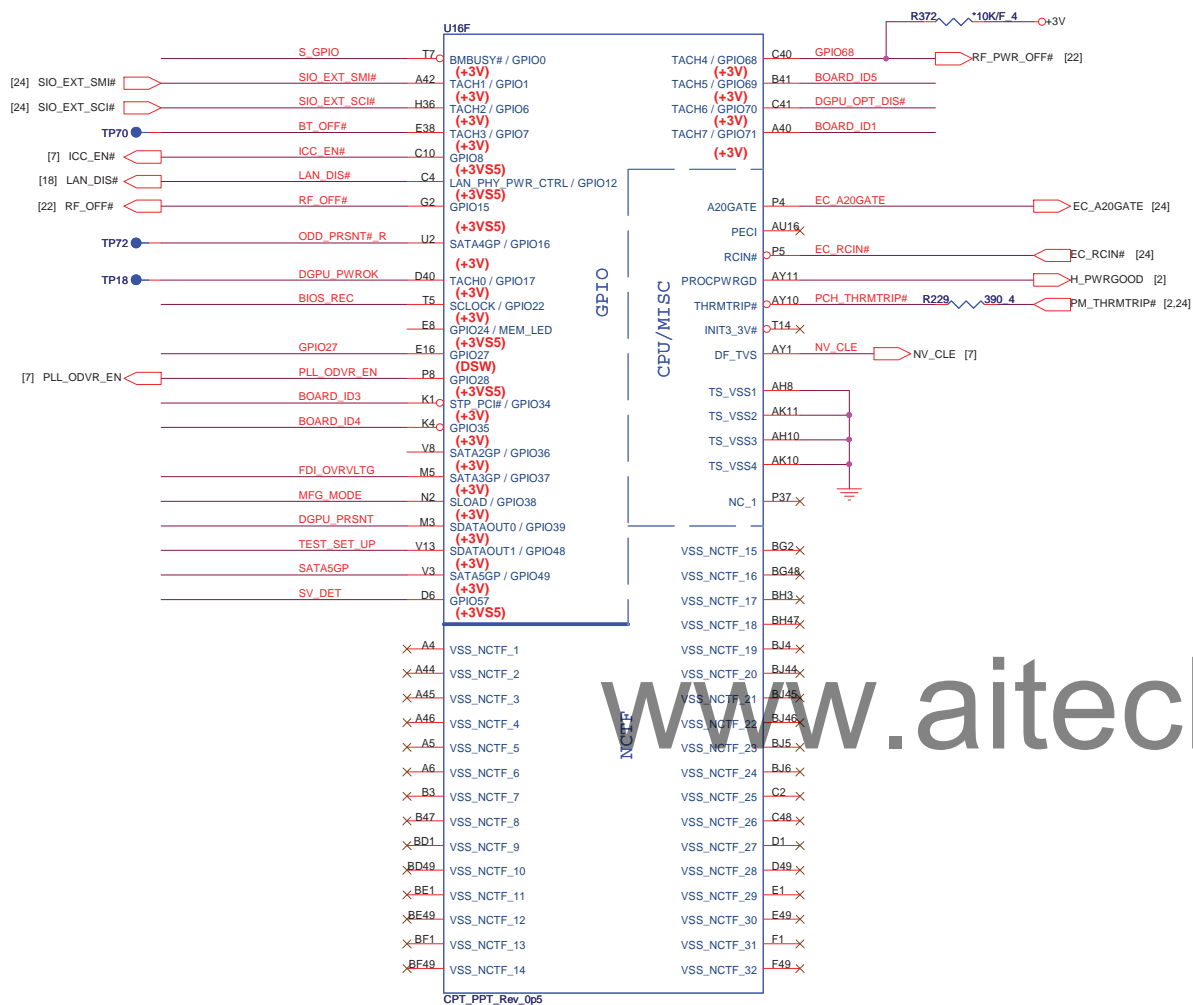
PCIE Clock



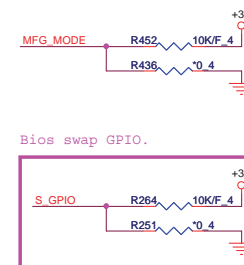
SMBus/Pull-up(CLG)



Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



MFG-TEST



Bios swap GPIO.

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

TEST_SET_UP (R248) (*10K/F 4) (+3V)

SV_SET_UP (R236) (*0.4) (+3V)

High = Strong (Default)

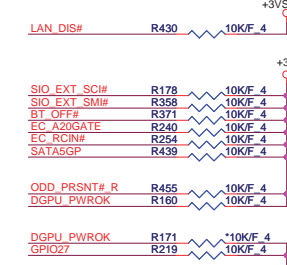
DGPU_PWR_EN_R pull high

+3V 200K, 200K 是不上件。

DMI TERMINATION VOLTAGE OVERRIDE

Reserved only

GPIO Pull-up/Pull-down(CLG)



BIOS RECOVERY

High = Disable (Default)

Low = Enable

TEST_DETECT (R244) (*100K/F 4) (+3V)

SV_DET (R257) (*10K/F 4) (+3V)

Low = Default

FDI TERMINATION VOLTAGE OVERRIDE

Reserved only

BOARD_ID[3:0]	Model Name
0000	QLGA
0001	TWC
0010	JW2
0011	T8D
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C

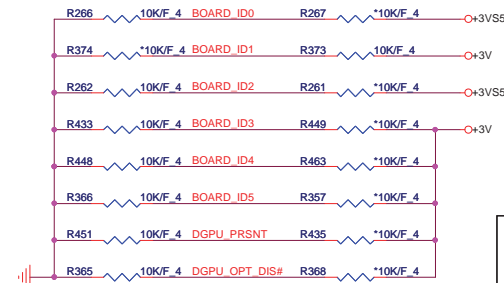
Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	No Dolby=0, Dolby=1
BOARD_ID5	GPIO69	HM76=0, HM70=1
DGPU_PRSN#	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

20110816 Define BRD_ID[3:0]

[8] BOARD_ID0 BOARD_ID0

[8] BOARD_ID2 BOARD_ID2



0804 Board_ID1 change to +3V

Board_ID5 change to +3V

[2,6,7,8,10,12,13,14,15,16,17,19,20,22,23,24,29,32,34]

[6,7,8,10,14,19,22,24,26,29,30,34]

+3V

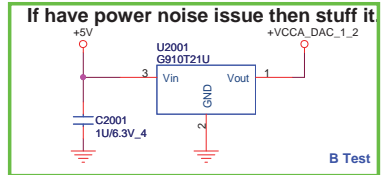
+3VSS



PROJECT : JW2

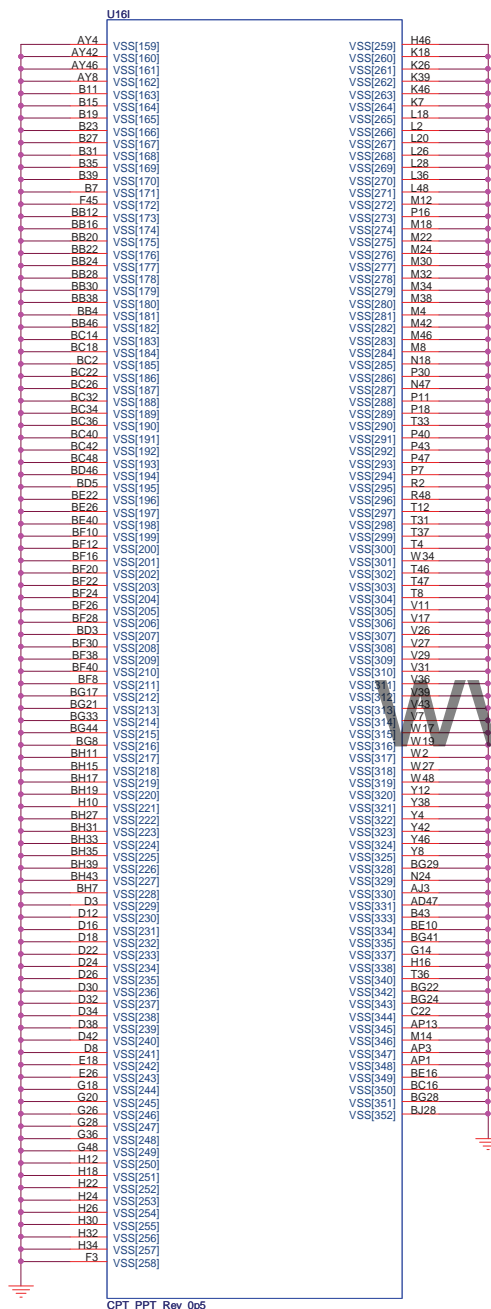
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO)	1A
Date: Tuesday, February 07, 2012	Sheet	9 of 34

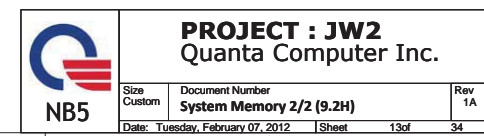


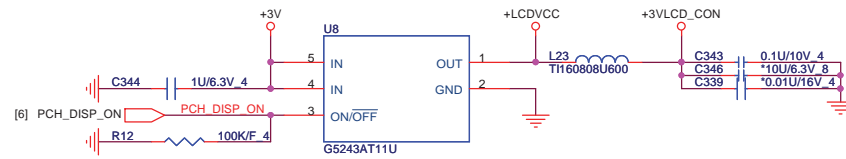
Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)

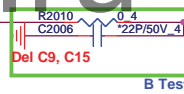
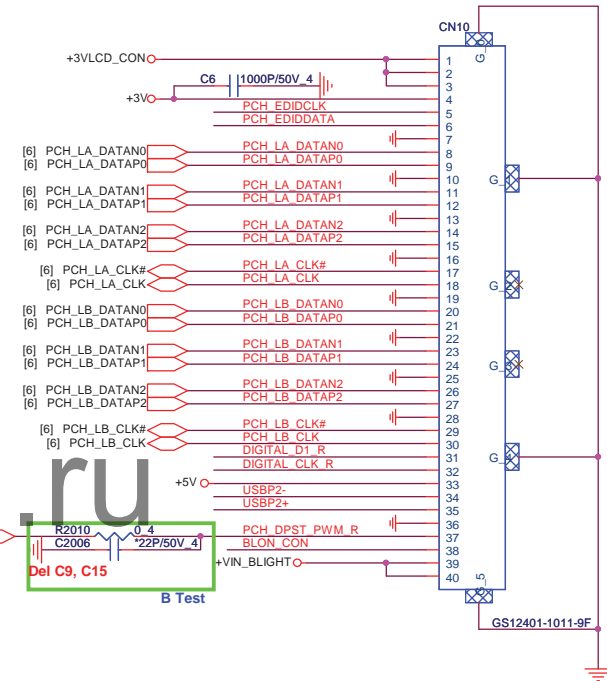
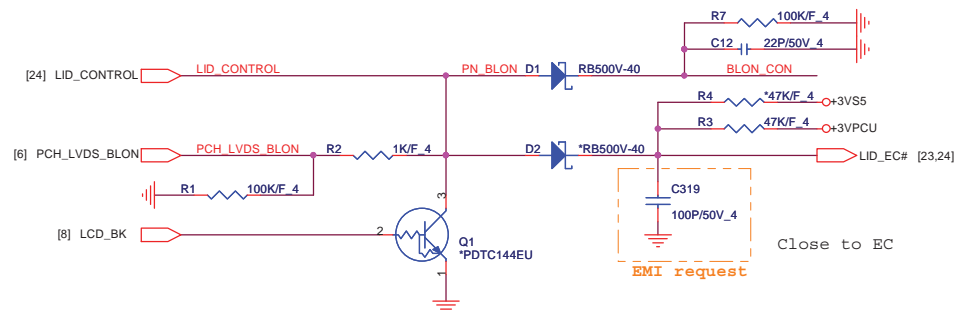
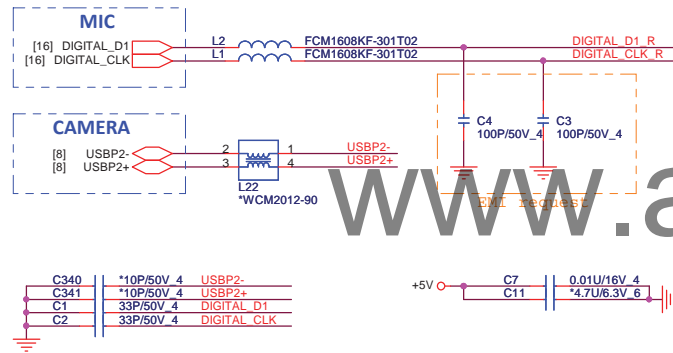








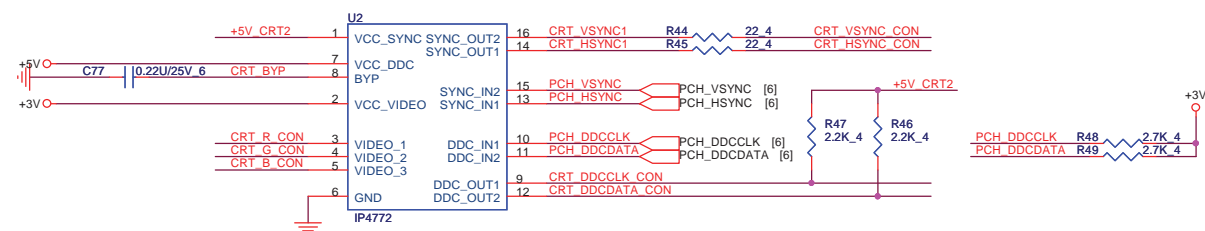
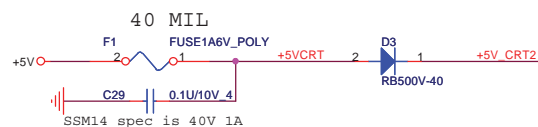
USB Camera Connector



PROJECT : JW2
Quanta Computer Inc.

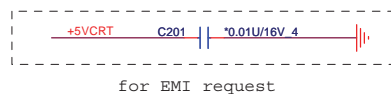
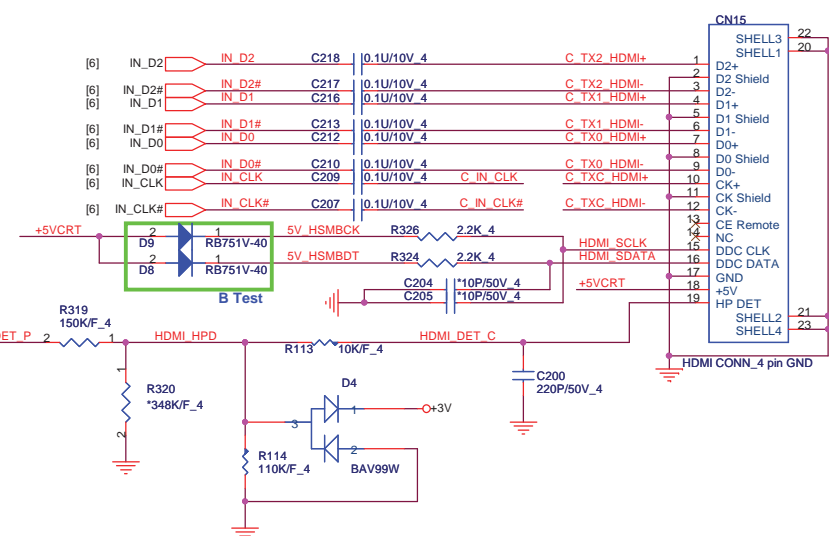
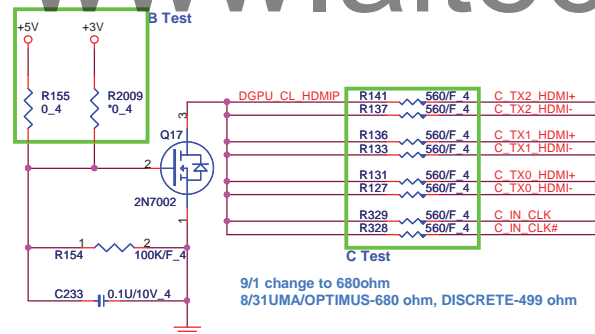
Size	Document Number	Rev
Custom	LCD Connector (LVDS)	1A
Date: Tuesday, February 07, 2012	Sheet 14 of 34	

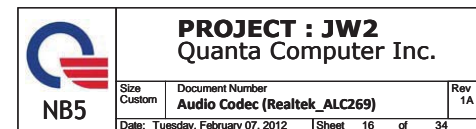
[2,6,7,8,9,10,12,13,15,16,17,19,20,22,23,24,29,32,34] +3V
[7,10,15,16,22,23,34] +5V
[19,25,26,27,29,33,34] +VIN
[7,19,22,23,24,25,26] +3VPCU

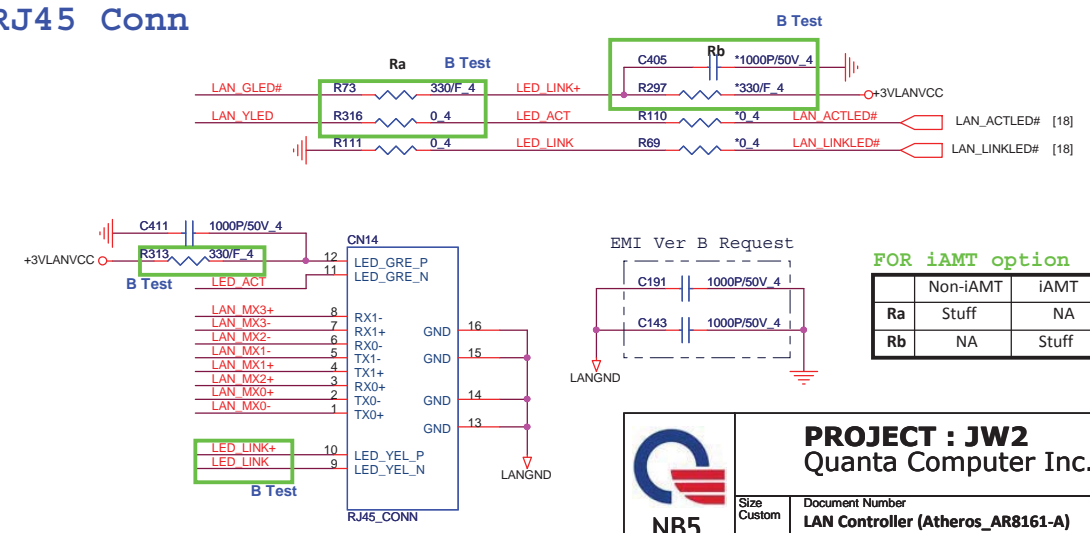
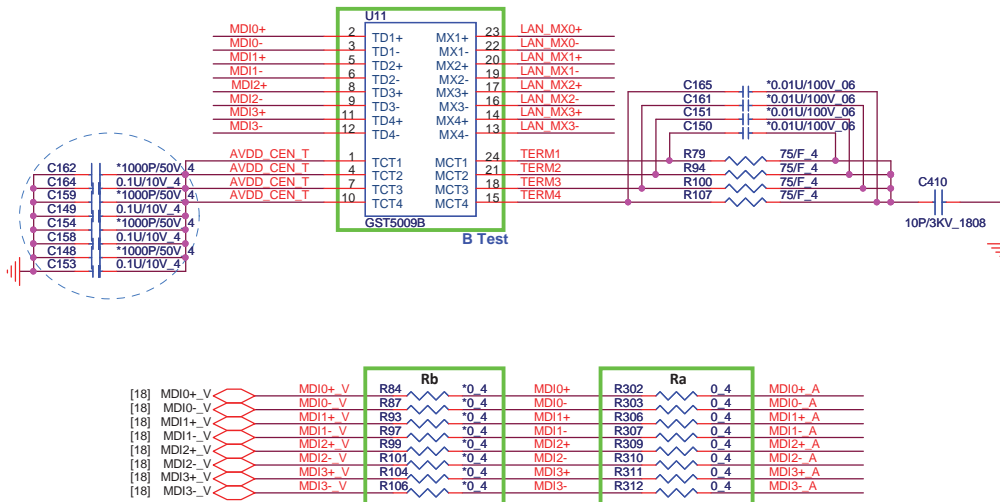
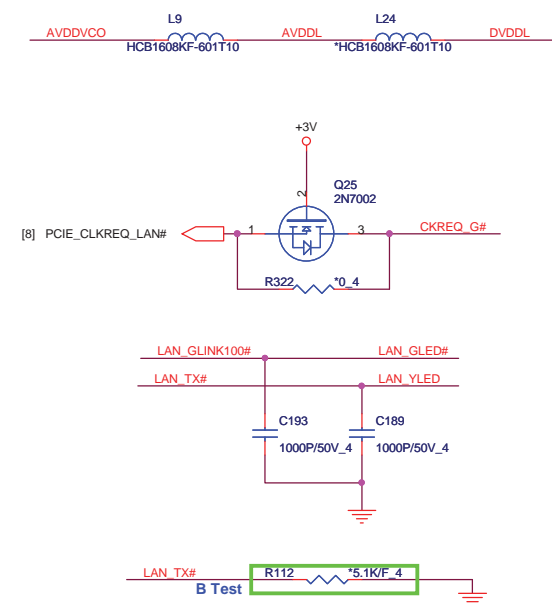
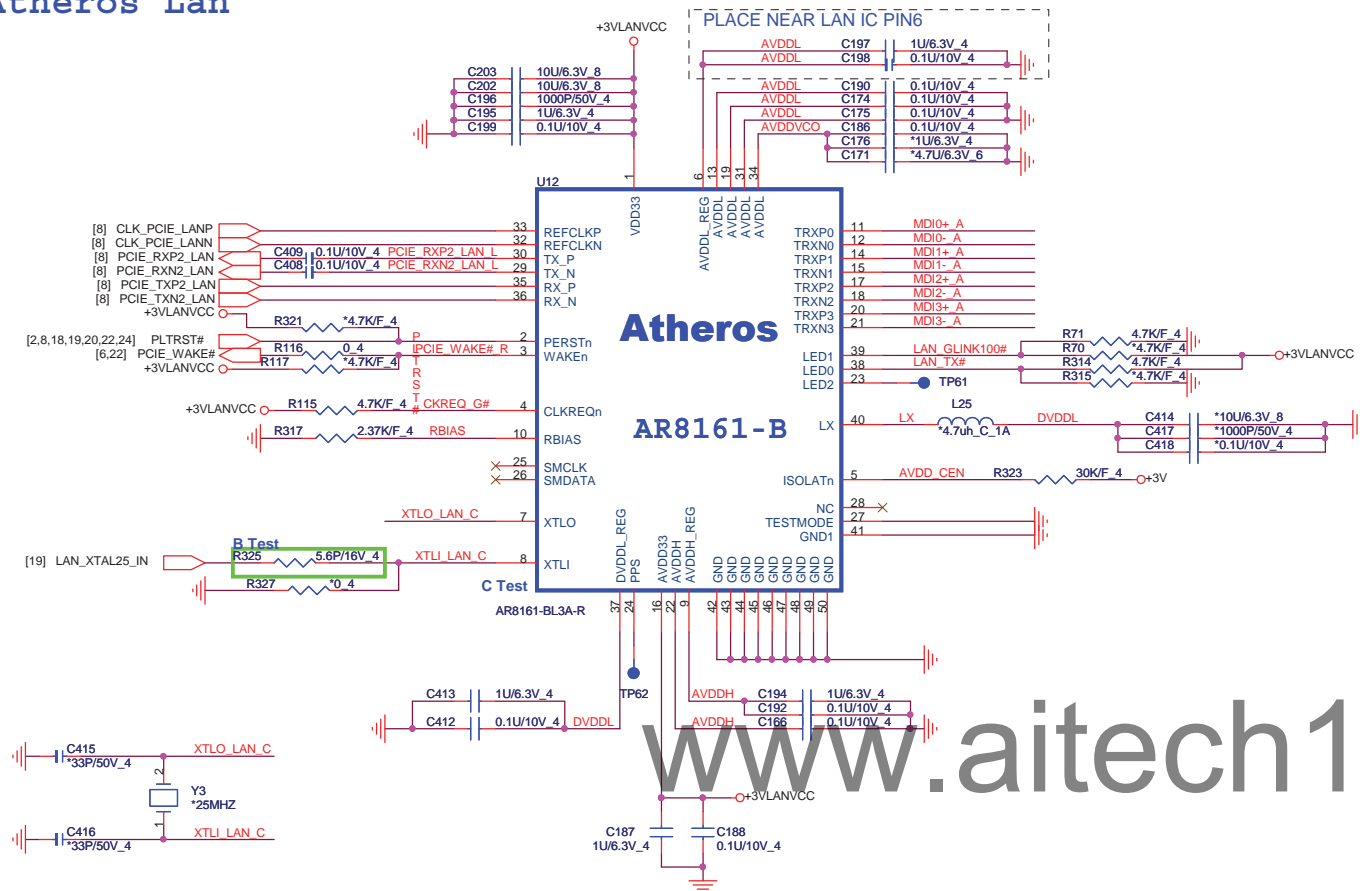


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HDMI PORT

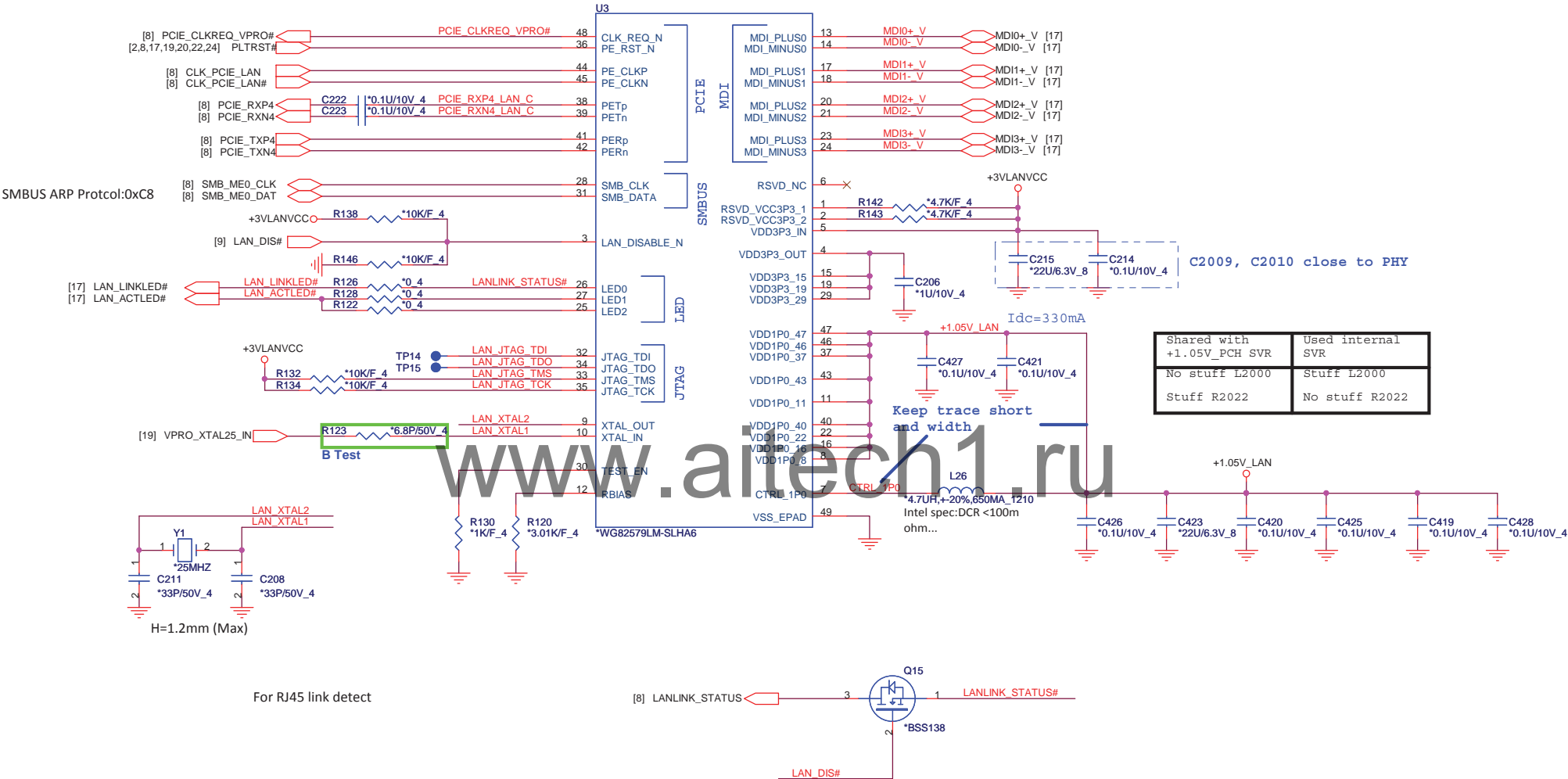






FOR iAMT option

	Non-iAMT	iAMT
Ra	Stuff	NA
Rb	NA	Stuff



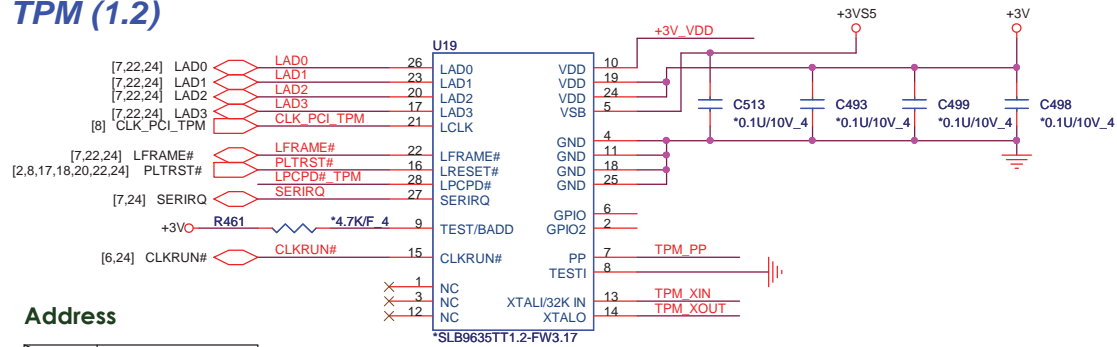
Shared with +1.05V_PCH SVR	Used internal SVR
No stuff L2000	Stuff L2000
Stuff R2022	No stuff R2022



PROJECT : JW2
Quanta Computer Inc.

Size B	Document Number Intel Lewisville 82579LM	Rev 1A
Date: Tuesday, February 07, 2012	Sheet 18 of 34	

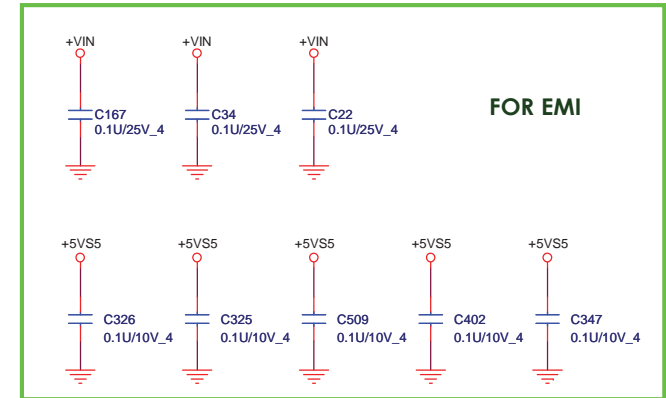
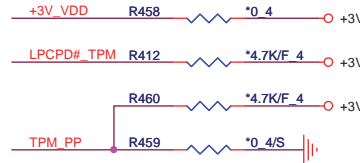
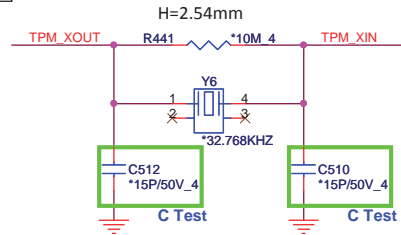
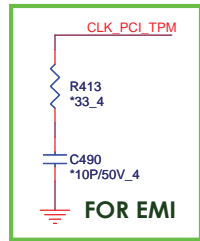
TPM (1.2)



Address

	BADD
HIGH	4EH/4F

(default)



FOR EMI

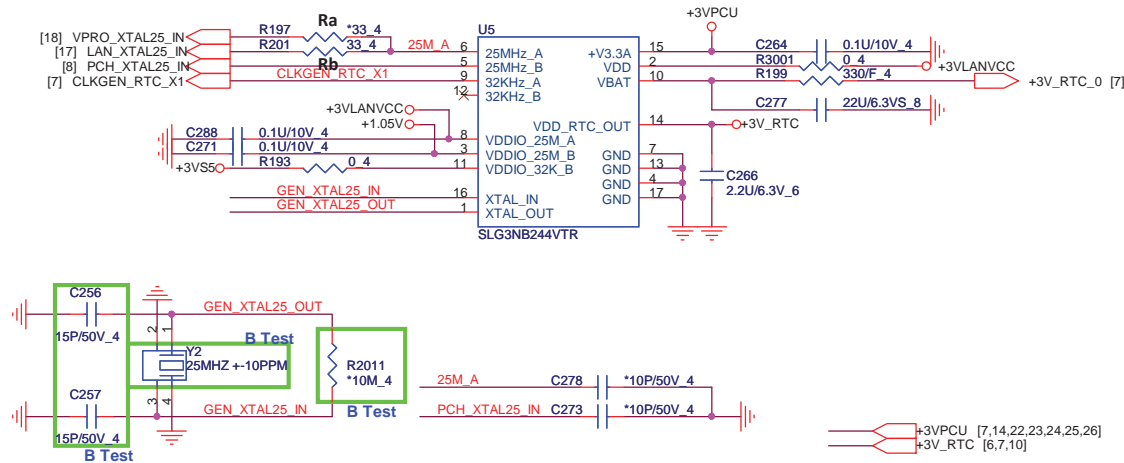
Green CLK

FOR LAN CLK option

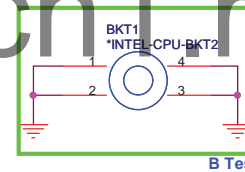
	Atheros	vPRO
Ra	NA	Stuff
Rb	Stuff	NA

FOR TPM option

	TPM	Non-TPM
R419	Stuff	NA
U5	AL3NB246000	AL3NB244000



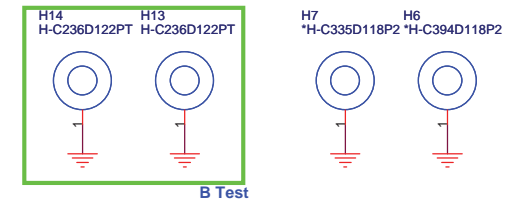
CPU Bracket



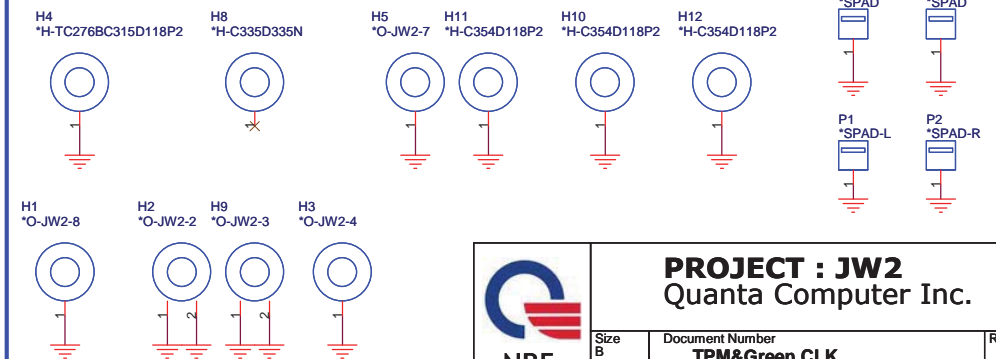
MINI PCI Pad



PCH NU Screw Hold



System Screw Hold

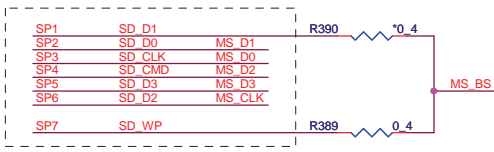
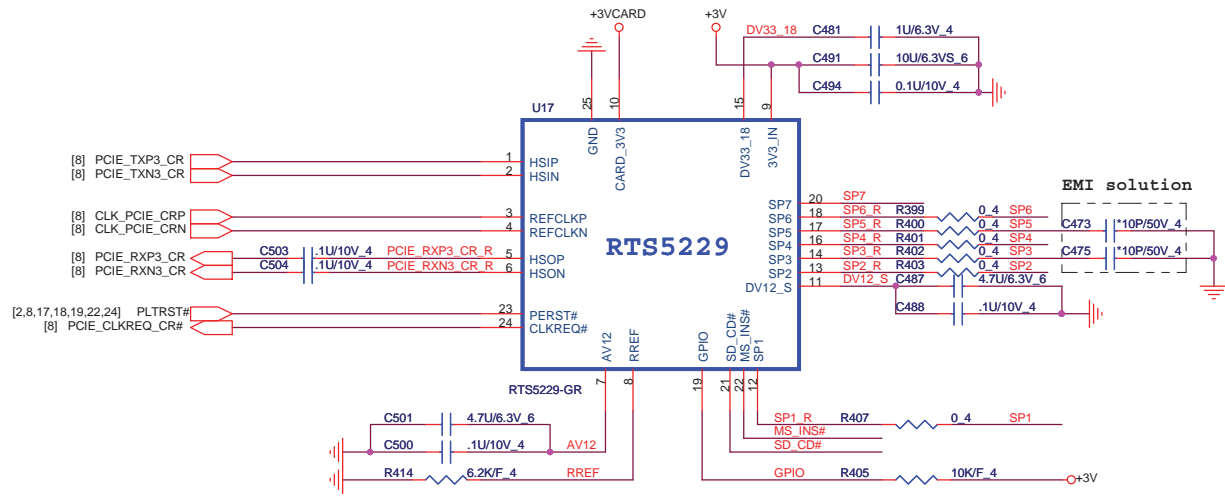


PROJECT : JW2
Quanta Computer Inc.

Size	Document Number	Rev
B	TPM&Green CLK	1A

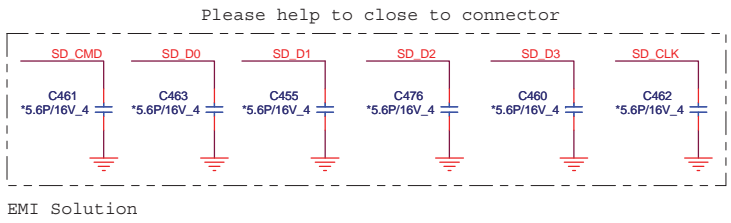
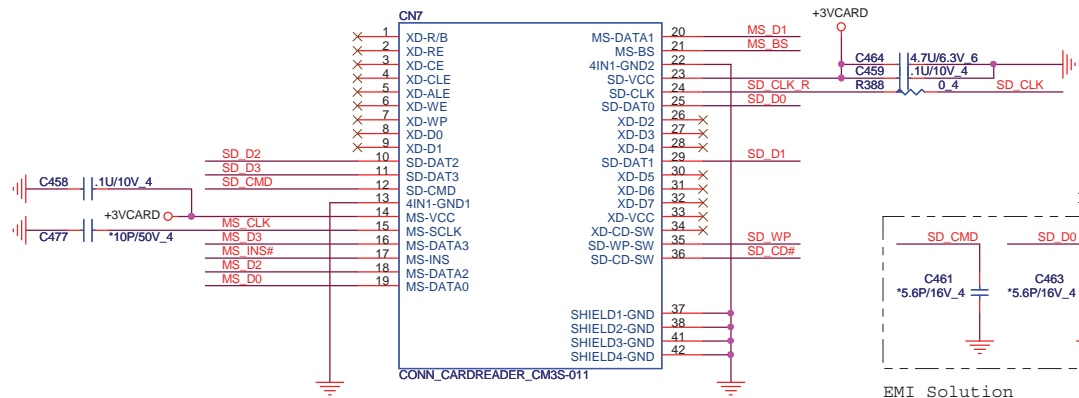
Date: Tuesday, February 07, 2012 Sheet 19 of 34

Share Pin




CR Socket

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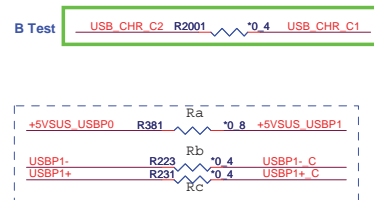
- Note:
- 1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
 - 2. C5265, C5202 close to U37 pin7
 - 3. C1021, C1022 close to U37 pin11
 - 4. C1089, C1090 close to U37 pin9
 - 5. C1019 close to U37 pin15
 - 6. C1026, C1027 close to CN27 pin11
 - 7. C1025 close to CN27 pin4



PROJECT : JW2
Quanta Computer Inc.

Size Custom	Document Number RTS5229 & CR SOCKET	Rev 1A
Date: Tuesday, February 07, 2012 Sheet 20 of 34		

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USB Charger option

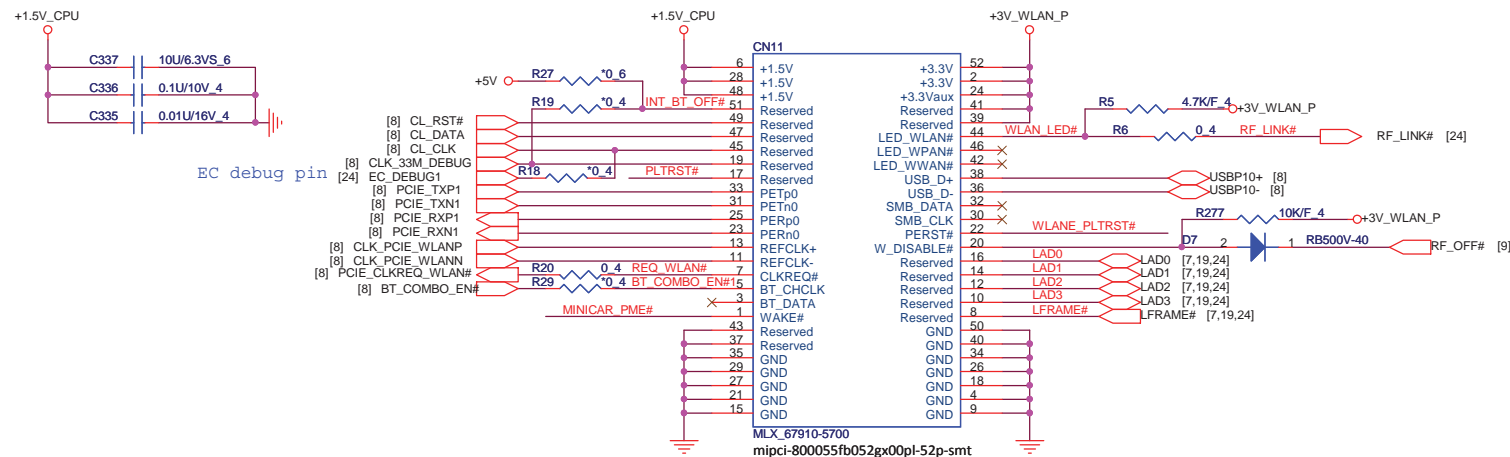
LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
charge mode	CDP	CDP	DCP	DCP
user define and wake up		SDP		OFF



PROJECT : JW2
Quanta Computer Inc.

Size Custom	Document Number USB 3.0 Connector	Rev 1A
Date: Tuesday, February 07, 2012		Sheet 21 of 34

Mini Card/WLAN/BT(Optional)

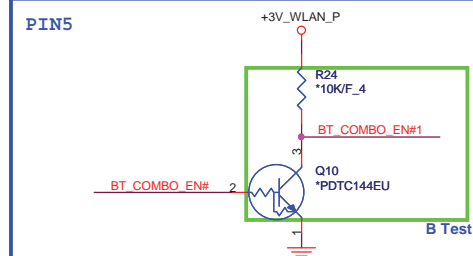
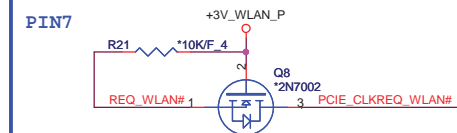
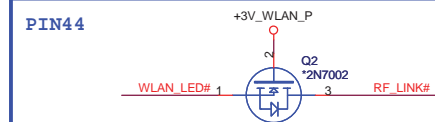


LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

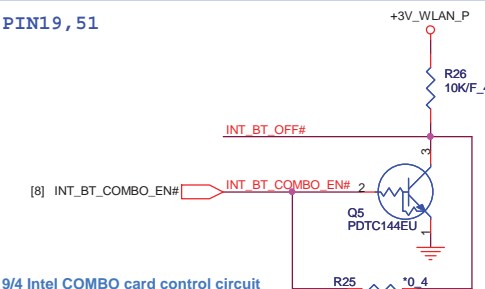
For EMI Suggestion



Avoid leakage issue



PIN19, 51



9/4 Intel COMBO card control circuit

1.add R1001,R1002,Q1001

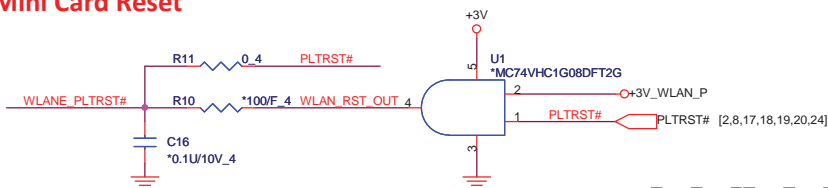
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"



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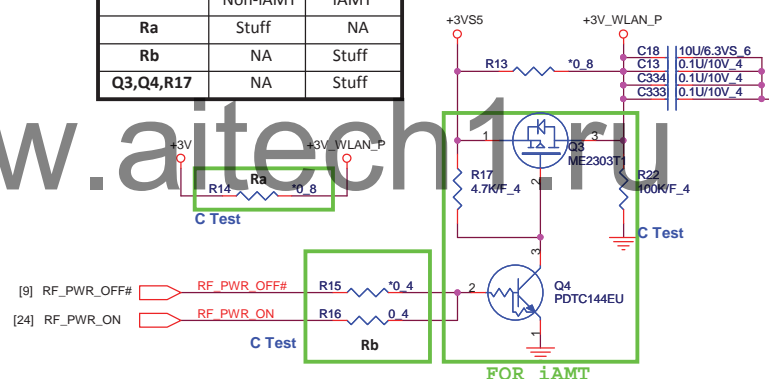
Size Custom	Document Number MINI PCIE CONN/LED	Rev 1A
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Mini Card Reset

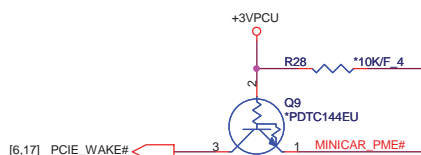


FOR iAMT option

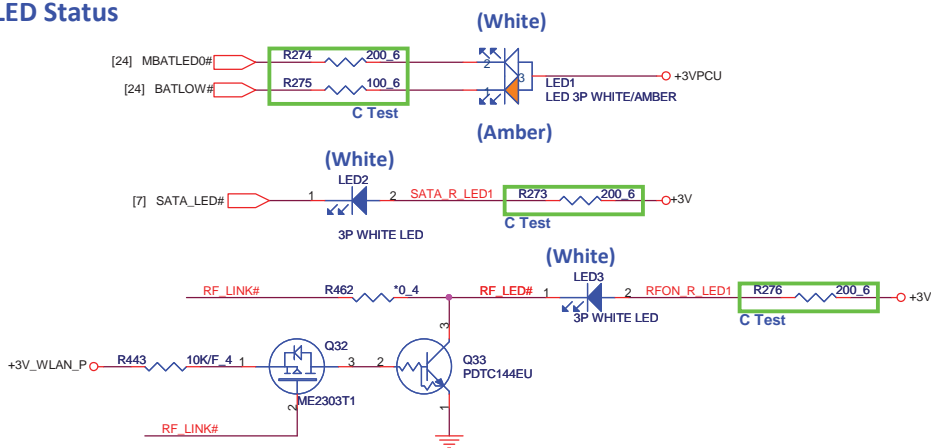
	Non-iAMT	iAMT
Ra	Stuff	NA
Rb	NA	Stuff
Q3,Q4,R17	NA	Stuff



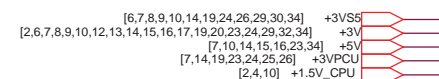
Support Wake Function(Reserve)



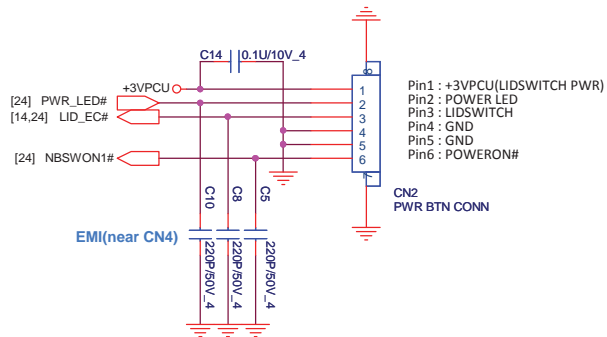
LED Status



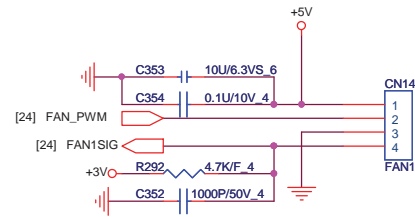
Capacity module Connector



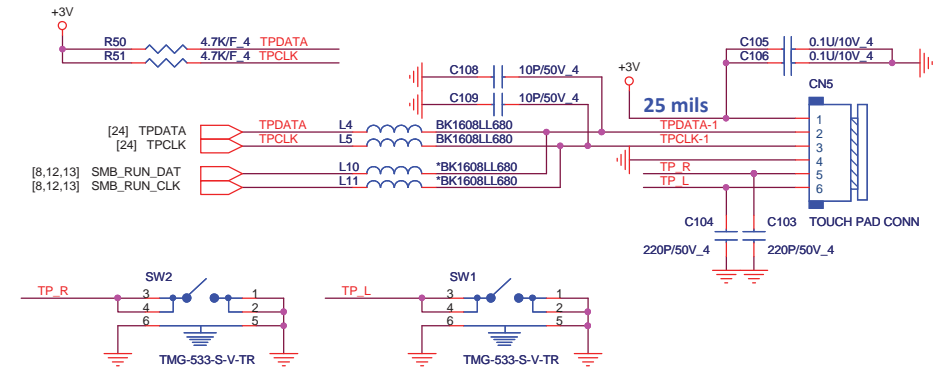
Power Button Connector



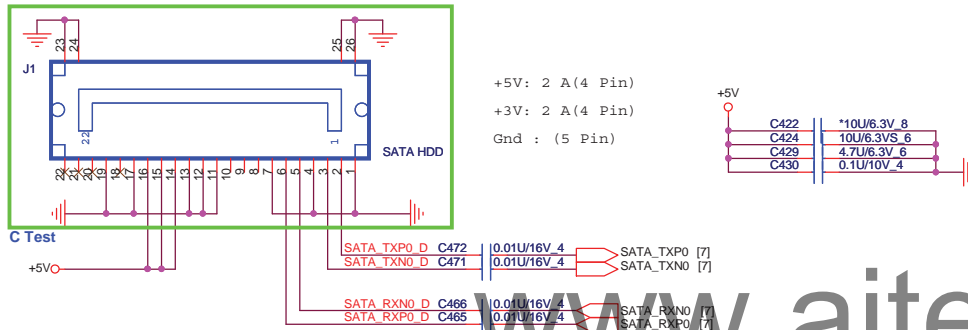
CPU FAN



Touch Pad Connector

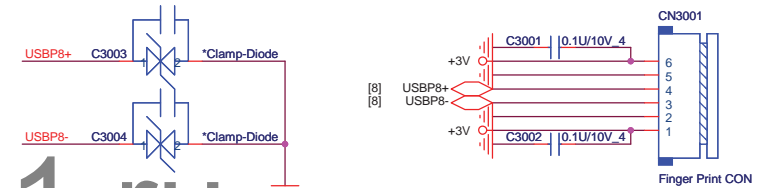


SATA HDD Connector

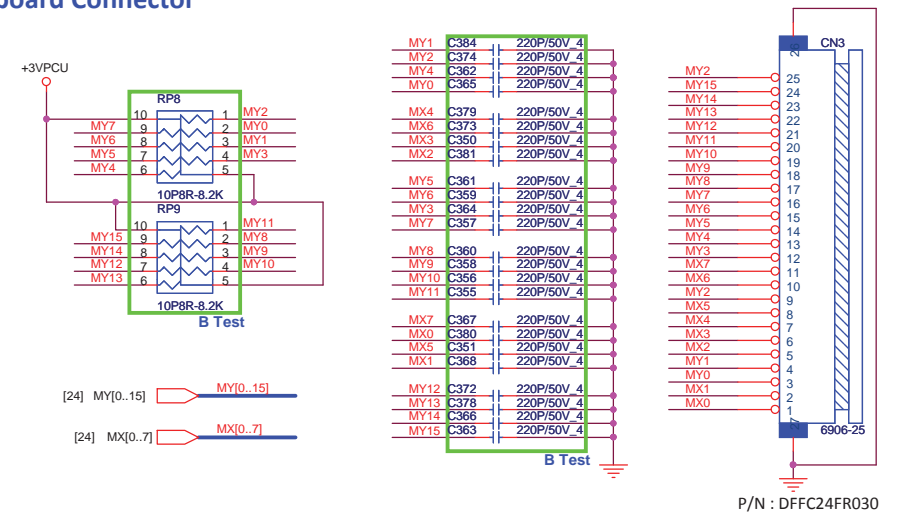


DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

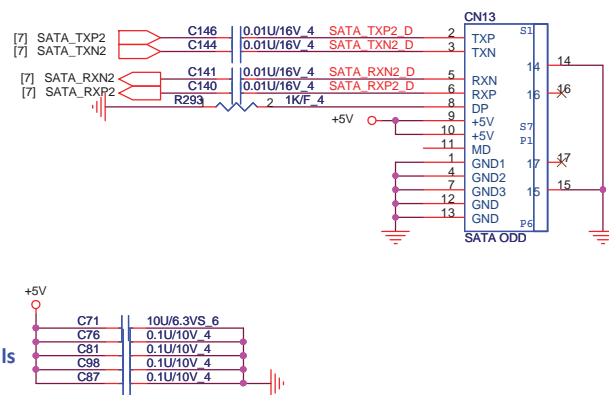
Finger Print Connector



Keyboard Connector



SATA ODD Connector

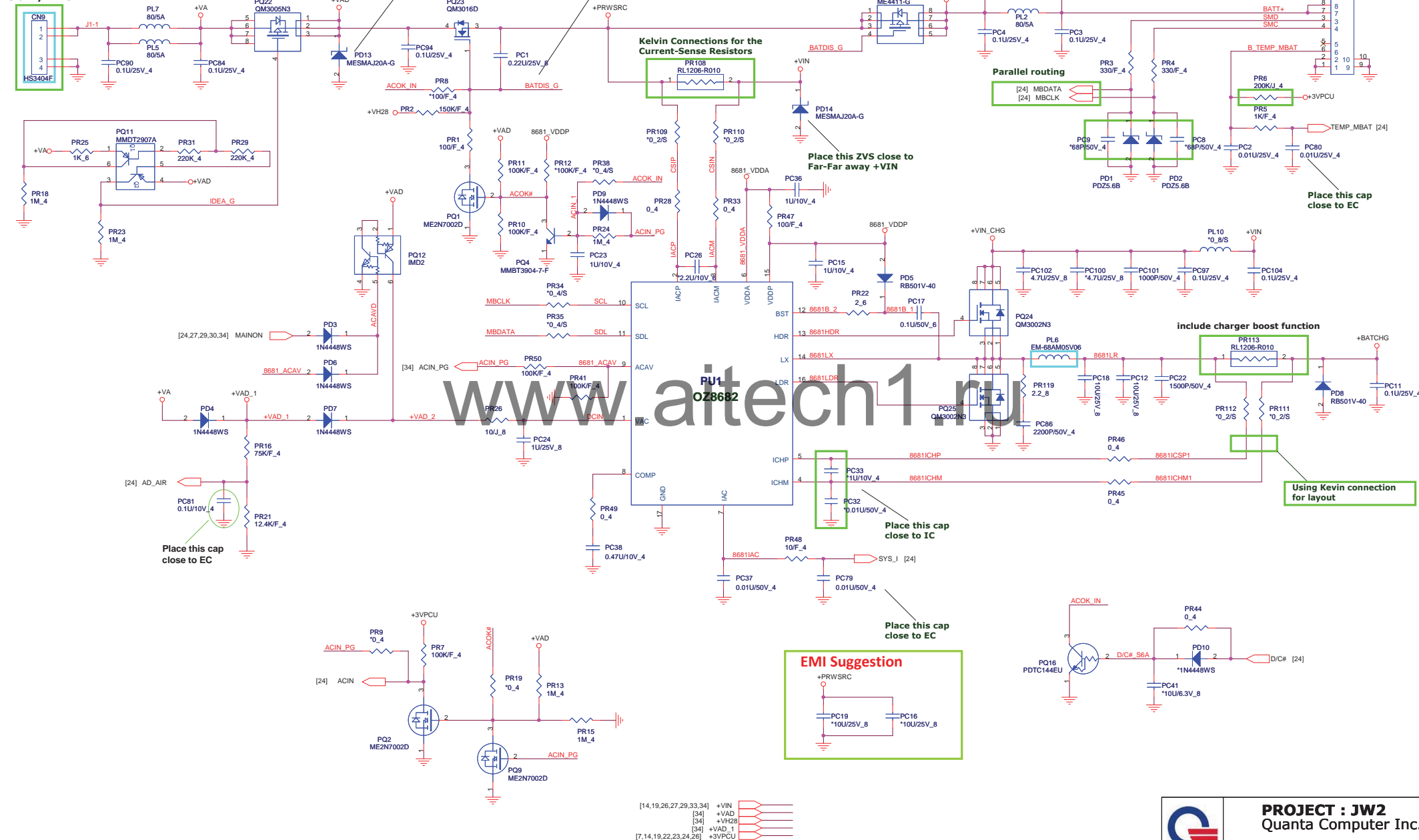


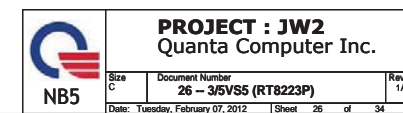
120 mils

[2,6,7,8,9,10,12,13,14,15,16,17,19,20,22,24,29,32,34] +3V
[7,10,14,15,16,22,34] +5V
[7,14,19,22,24,25,26] +3VPCU

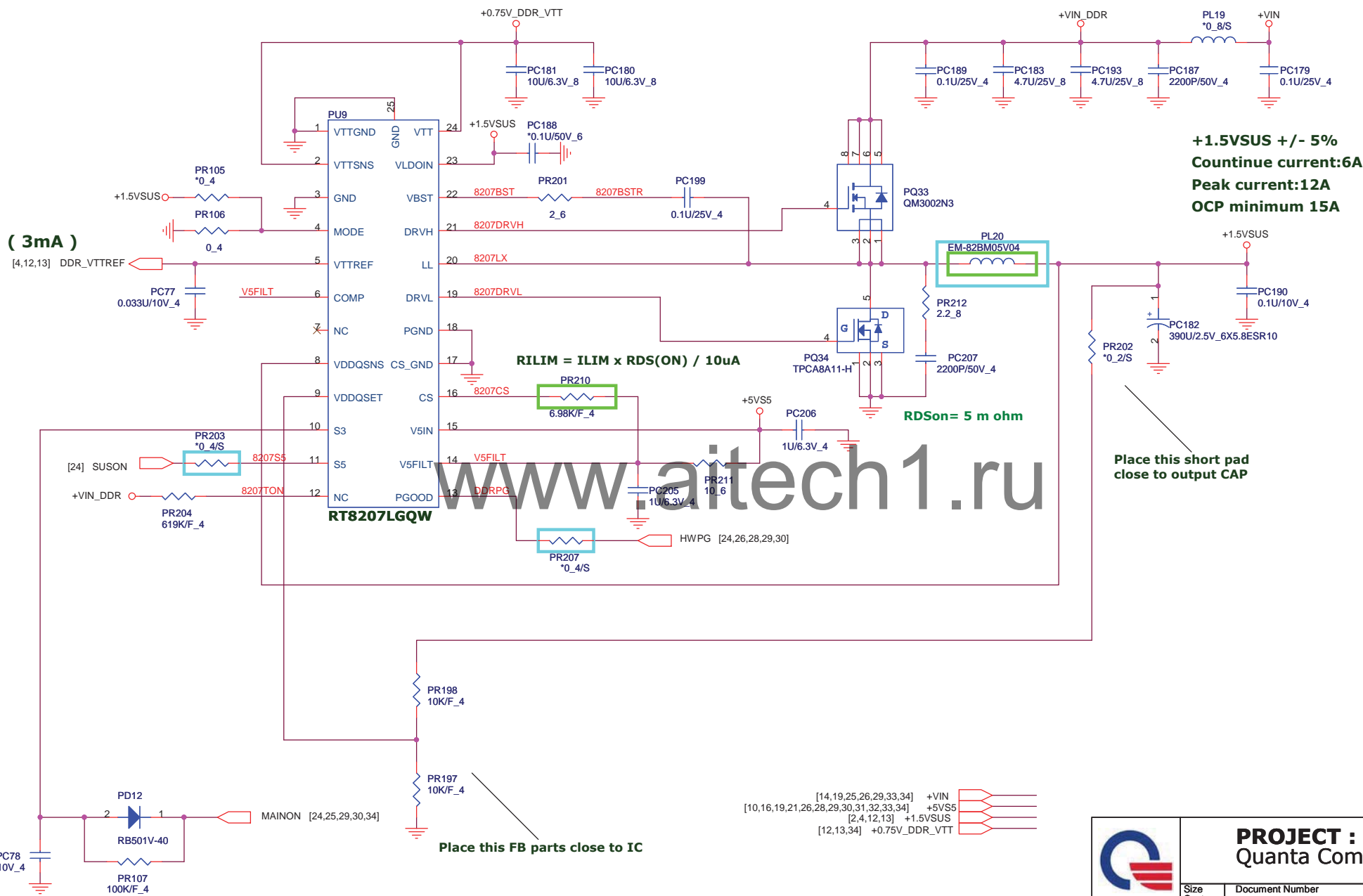


TOP DC_JACK
90W/4.75A





(VTT/2A)



+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

**Place this short pad
close to output CAP**

Place this FB parts close to IC

[14,19,25,26,29,33,34]	+VIN	
[10,16,19,21,26,28,29,30,31,32,33,34]	+5VS5	
[2,4,12,13]	+1.5VSUS	
[12,13,34]	+0.75V_DDR_VTT	

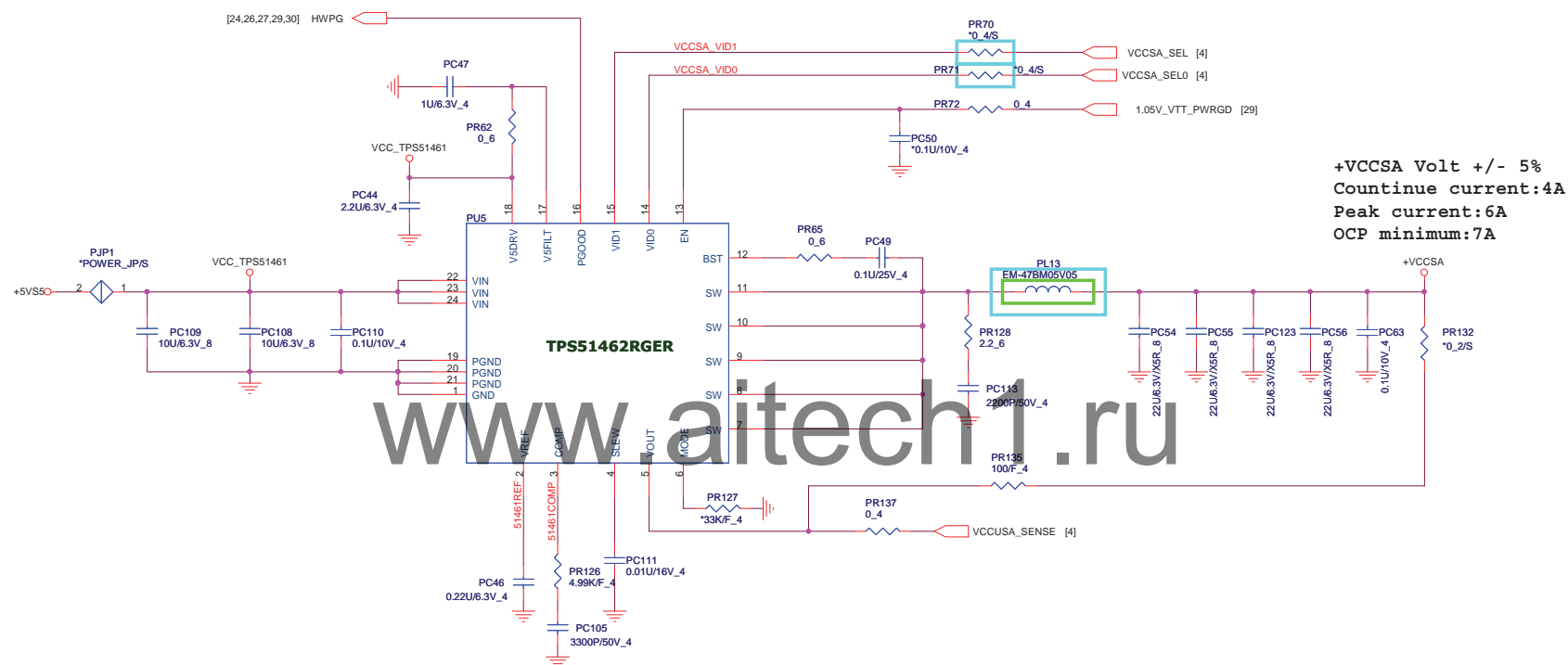


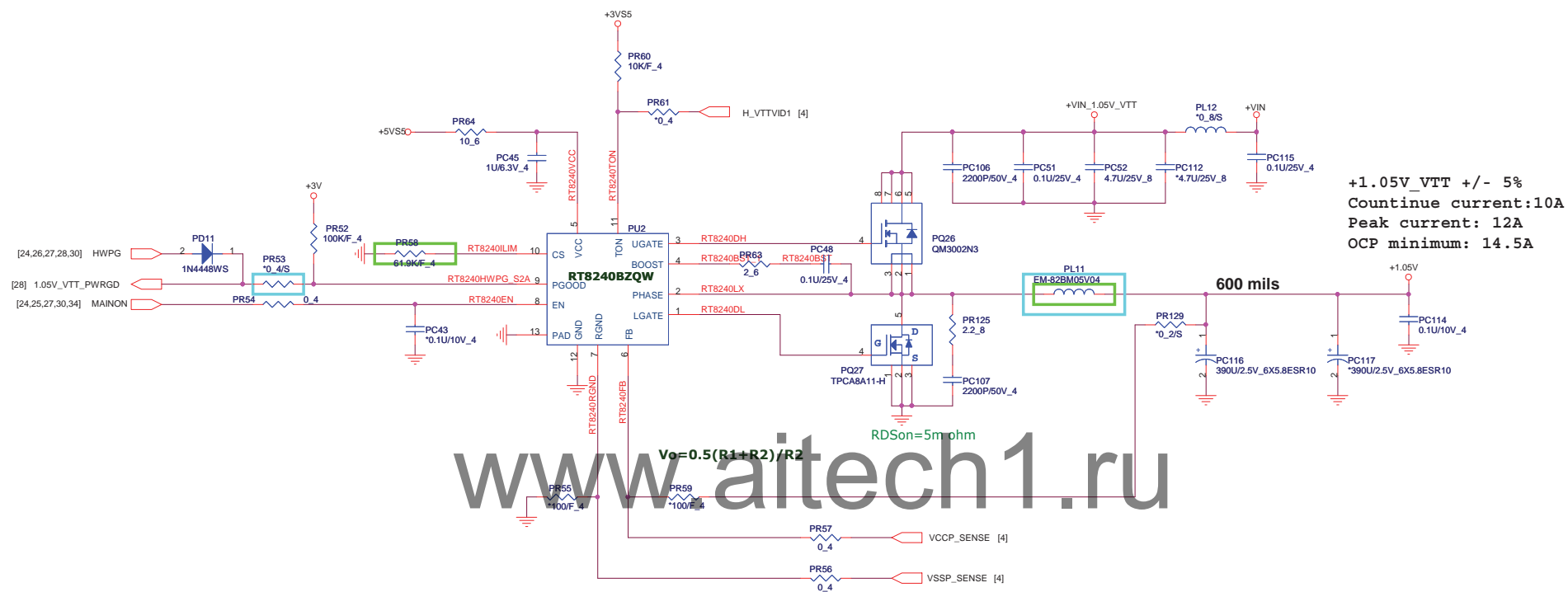
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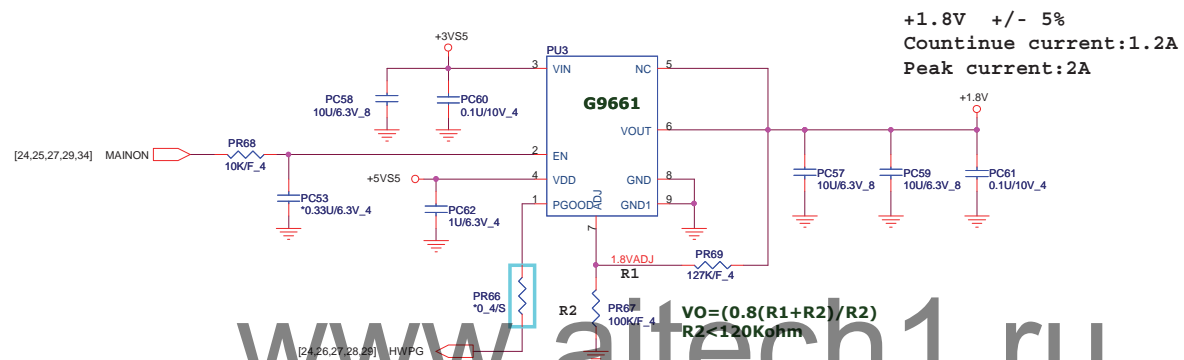
Size Custom	Document Number 27 -- DDR3 (RT8207)	Rev 1A
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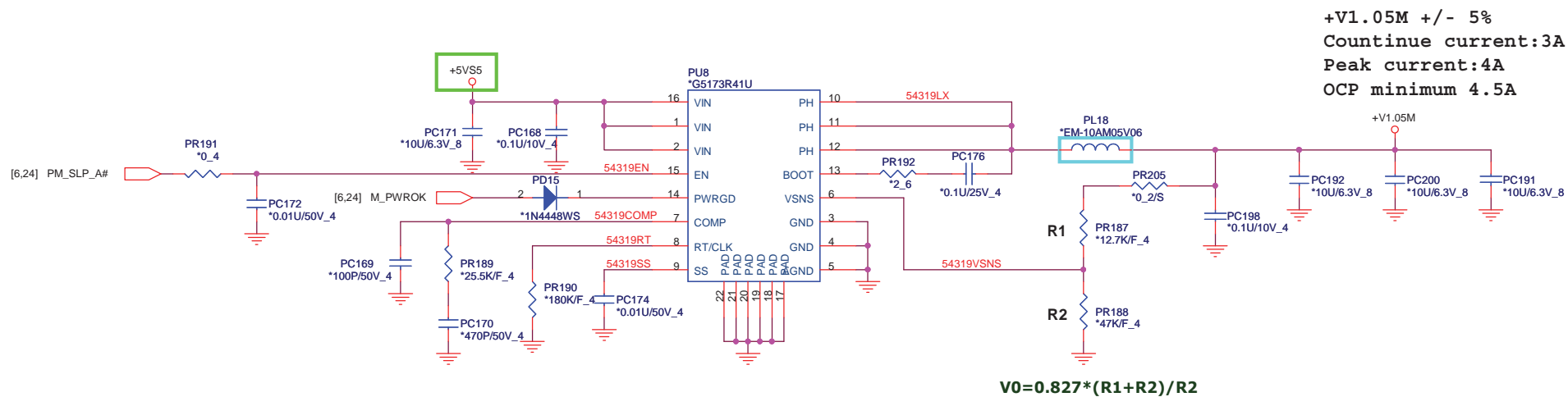
CPU system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V







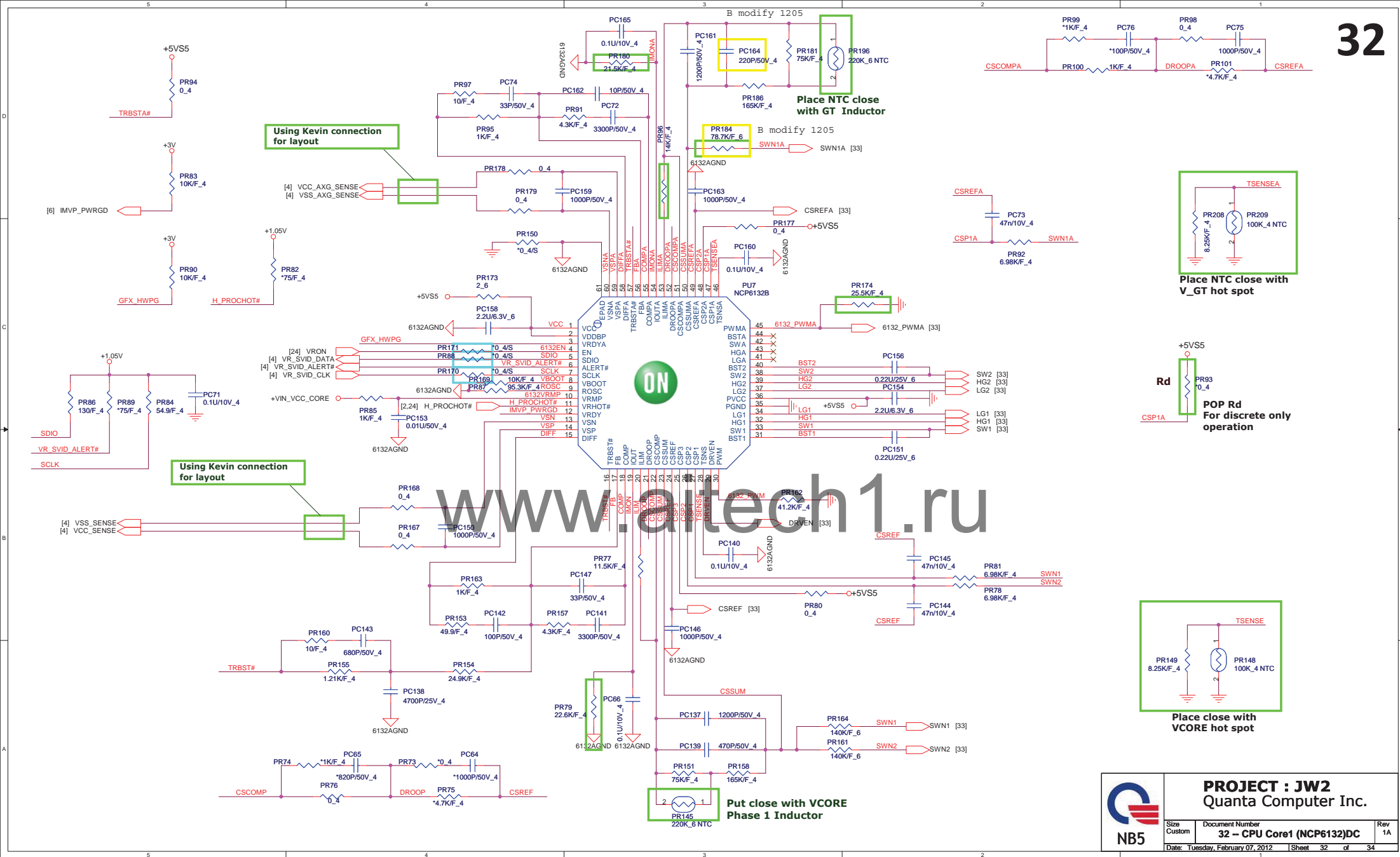


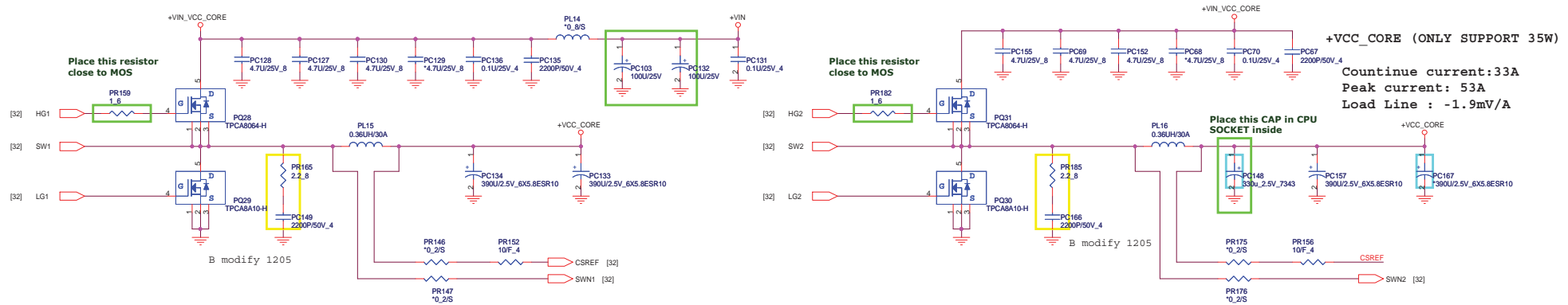
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Size B	Document Number 31 -- +V1.05M (G5173)	Rev 1A
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